16. The ink-jet recording apparatus according to claim 14, further comprising a driving circuit for performing the recording and the circuit blocks each respectively output a signal for initializing the driving circuit.

17. (Twice Amended) A control method of an integrated-circuit apparatus having a CPU and a plurality of circuit blocks to be initialized in accordance with external reset signals, comprising the steps of:

initializing the circuit blocks;

outputting an initialization completion signal for communicating completion of initialization in the initializing step;

outputting an enable signal for permitting operations of the circuit blocks in accordance with the signal output in the initialization completion signal outputting step; and

permitting the circuit blocks to perform the operations by the enable signal and the external reset signals.

REMARKS

Reconsideration and withdrawal of the objection and rejections set forth in the above-mentioned Official Action in view of the foregoing amendments and the following remarks are respectfully requested.

Claims 1-17 remain pending in the application. Claims 1, 14 and 17 are independent and have been amended herein.

Applicant notes with appreciation the indication that Claims 5, 6, 7/5-6, 8/5-6, 9/7/5-6, 10/5-6, 15 and 16 recite allowable subject matter. These claims were objected to for being dependent upon rejected base claims. However, these claims will not be rewritten in independent form at this time because their respective independent claims are believed to be allowable for the reasons discussed below.

Claims 1-4, 7/1-4 and 17 were rejected under 35 U.S.C. § 102 over Japanese Patent Laid-Open Application No. 2001-100873 (Hoshino). Claims 8/1-4, 9/7/1-4, 10/1-4, 11/7/1-4, 12/8/1-4 and 13/9/7/1-4 were rejected under 35 U.S.C. § 103 as being unpatentable over Hoshino in view of U.S. Patent No. 5,929,672 (Mitani). Claim 14 was rejected under § 103 as being unpatentable over U.S. Patent No. 5,784,080 (Nitta et al.) in view of Hoshino. These rejections are respectfully traversed.

Independent Claim 1 is directed to an integrated-circuit apparatus and independent Claim 14 is directed to an ink-jet recording apparatus comprising an integrated-circuit apparatus. The integrated-circuit apparatus comprises a CPU and a plurality of circuit blocks to be initialized in accordance with external reset signals. The circuit blocks each respectively output an initialization completion signal for communicating completion of initialization after the circuit blocks are initialized. The CPU outputs an enable signal for permitting operations of the circuit blocks in accordance with the initialization completion signals output from the circuit blocks. The circuit blocks are permitted to perform operations by the enable signal and the external reset signals.

As is recited in independent Claim 17, the present invention relates to a control method of an integrated-circuit apparatus having a CPU and a plurality of circuit

blocks to be initialized in accordance with external reset signals. The method includes the steps of initializing the circuit blocks, outputting an initialization completion signal for communicating completion of initialization in the initializing step, outputting an enable signal for permitting operations of the circuit blocks in accordance with the signal output in the initialization completion signal outputting step and permitting the circuit blocks to perform the operations by the enable signal and the external reset signals.

With the above arrangements and methods, a CPU and a plurality of circuit blocks can be initialized in accordance with external reset signals. After receiving these external reset signals, and in accordance with initialization completion signals output from circuit blocks, the CPU can output an enable signal for permitting operations of the circuit blocks. That is, the circuit blocks are permitted to perform the operations by the enable signal and the external reset signals, and by permitting the operations of the circuit blocks, resetting can be considered to be cancelled.

Support for the foregoing features can be found in the original specification at least at page 10, lines 6-17. For example, signals S6 and S19 in Figs. 5 and 6 become H level and signal S21 is output to cancel the resetting of logic circuits 3 and 4.

As described previously, Hoshino relates to an initial setting processing circuit for a line card. A first discriminating circuit outputs an initial setting start signal for starting initial setting processing of the device inside the line card, and an initial setting circuit receives the initial setting start signal, performs initial setting processing of the device inside the line card and outputs an initialization state signal showing whether

relevant initial setting processing has been successful. A second discriminating circuit outputs a setting end signal to the CPU based on the initialization state signal.

Applicant respectfully submits that Hoshino does not describe that reset signals are input into the CPU and the circuit blocks. Accordingly, Hoshino fails to disclose or suggest a CPU and a plurality of circuit blocks to be initialized in accordance with external reset signals, as is recited in independent Claims 1, 14 and 17.

Further, Hoshino does not disclose or suggest that the CPU outputs an enable signal for permitting operations of the circuit blocks in accordance with the initialization completion signals output from the circuit blocks, such that the circuit blocks are permitted to perform the operations by the enable signal and the external reset signals, as is recited in independent Claims 1 and 14. Likewise, Hoshino does not disclose or suggest outputting an enable signal for permitting operations of the circuit blocks in accordance with the signal output and initialization completion signal outputting step and permitting the circuit blocks to perform the operations by the enable signal and the external reset signals, as is recited in independent Claim 17.

Thus, Hoshino fails to disclose or suggest important features of the present invention recited in the independent claims.

Mitani describes a power-on reset circuit which does not output a reset signal when the source voltage drops momentarily for a time duration shorter than a specified duration. Nitta et al. describes a serial printer which performs an initializing operation after a waiting time has elapsed. However, these citations are not believed to remedy the deficiencies of Hoshino noted above with respect to the independent claims.

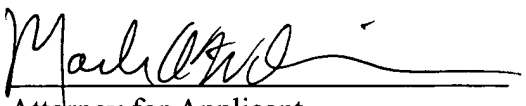
Thus, independent Claims 1, 14 and 17 are patentable over the citations of record. Reconsideration and withdrawal of the §§ 102 and 103 rejections are respectfully requested.

For the foregoing reasons, Applicant respectfully submits that the present invention is patentably defined by independent Claims 1, 14 and 17. Dependent Claims 2-13, 15 and 16 are also allowable, in their own right, for defining features of the present invention in addition to those recited in their respective independent claims. Individual consideration of the dependent claims is requested.

Applicant submits that the present application is in condition for allowance. Favorable reconsideration, withdrawal of the objection and rejections set forth in the above-noted Office Action, and an early Notice of Allowance are requested.

Applicant's undersigned attorney may be reached in our Washington, D.C. office by telephone at (202) 530-1010. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE TO CLAIMS

1. (Twice Amended) An integrated-circuit apparatus comprising:

a CPU[;] and a plurality of circuit blocks to be initialized in accordance with external reset signals, wherein

the circuit blocks each respectively output an initialization completion signal for communicating completion of initialization after the circuit blocks are initialized, [and]

the CPU outputs an enable signal for permitting operations of the circuit blocks in accordance with the initialization completion signals output from the circuit blocks, and

the circuit blocks are permitted to perform the operations by the enable signal and the external reset signals.

14. (Twice Amended) An ink-jet recording apparatus comprising:

an integrated-circuit apparatus for controlling recording using a recording head, wherein

the integrated-circuit apparatus comprises a CPU and a plurality of circuit blocks to be initialized in accordance with external reset signals,

the circuit blocks each respectively output an initialization completion signal for communicating completion of initialization after the circuit blocks are initialized, [and]

the CPU outputs an enable signal for permitting operations of the circuit blocks in accordance with the initialization completion signals output from the circuit blocks, and

the circuit blocks are permitted to perform the operations by the enable signal and the external reset signals.

17. (Twice Amended) A control method of an integrated-circuit apparatus having a CPU and a plurality of circuit blocks to be initialized in accordance with external reset signals, comprising the steps of:

initializing the circuit blocks;

outputting an initialization completion signal for communicating completion of initialization in the initializing step; [and]

outputting an enable signal for permitting operations of the circuit blocks in accordance with the signal output in the initialization completion signal outputting step; and

permitting the circuit blocks to perform the operations by the enable signal and the external reset signals.

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